CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A data communication system, comprising:

a first integrated circuit; and

a second integrated circuit coupled for source synchronous communication with the first integrated circuit;

the second integrated circuit including a recapture circuit, the recapture circuit configured to perform internally timed transfers of data, the data obtainable from the first integrated circuit in association with a source clock domain, the internally timed transfers of the data being from the source clock domain into an internal clock domain of the second integrated circuit;

wherein the internally timed transfers of data are responsive to a timing signal of the source clock domain from the first integrated circuit and an internal clock signal of the internal clock domain of the second integrated circuit

wherein the recapture circuit comprises:

a first data registration stage configured to capture the data in the source clock domain;

a data valid signal generator configured to provide a valid data signal responsive to the internal clock signal and a derived signal from the timing signal; and

a second data registration stage configured to recapture the data in the internal clock domain responsive to the data valid signal and the internal clock signal

wherein the derived signal is provided by dividing frequency of the timing signal.

2-4. (Canceled)

5. (Currently Amended) The system, according to claim [[4]]1, wherein the derived signal is used as an enable signal for the first data registration stage.

6. (Original) The system, according to claim 5, wherein the derived signal is used as a data input signal to the data valid signal generator.

7. (Currently Amended) The system, according to claim [[3]]1, wherein the frequency of the timing signal is at least approximately twice the frequency of the derived signal.

8. (Currently Amended) The system, according to claim [[3]]1, wherein the data valid signal generator is configured to provide the data valid signal by combining two transfer done signals.

9. (Original) The system, according to claim 8, wherein one of the two transfer done signals leads the other one of the two transfer done signals.

10. (Original) The system, according to claim 1, wherein the second integrated circuit comprises a digital clock module, the digital clock module coupled to receive a clock signal of the internal clock domain and configured to provide a plurality of clock signals, the plurality of clock signals being phases of the clock signal.

11. (Original) The system, according to claim 10, wherein the phases of the clock signal are at 0, 90, 180 and 270 degrees to provide the plurality of clock signals.

12. (Original) The system, according to claim 1, wherein at least one of the first and second integrated circuits comprises a programmable logic device.

13. (Original) The system, according to claim 1, wherein the recapture circuit comprises a plurality of first-in, first-out buffers, each first in, first out buffer responsive to a timing signal of the source clock domain from the first integrated circuit and to an enable signal derived from the timing signal.

14. (Original) A recapture circuit, comprising:

a data capture stage including:

a first plurality of registers, the first plurality of registers coupled to receive a data signal and a timing signal and configured to capture data into a clock domain of the timing signal;

a frequency divider coupled to receive the timing signal and configured to provide an enable signal, the enable signal having a frequency less than the frequency of the timing signal;

the first plurality of registers coupled to receive the enable signal;

the first plurality of registers configured to provide a plurality of data phases, each of the data phases active on one of a leading edge or a lagging edge of the timing signal and one of high state or low state of the enable signal;

a data validity stage including:

a second plurality of registers, an input portion of the second plurality of registers coupled to receive the enable signal and an internal clock signal and configured to clock off of different edges of the internal clock signal, an output portion of the second plurality of registers coupled in series to the input portion and configured to clock off of different edges of the internal clock signal different from the input portion clockage;

a logical operator coupled to receive output from the second plurality of registers and configured to provide a data valid signal therefrom; and

a data recapture stage including:

a third plurality of registers, the third plurality of registers clocked responsive to the internal clock signal and write enabled responsive to the data valid signal, the third plurality of registers coupled to the first plurality of registers to receive output data therefrom and configured to recapture the output data into a clock domain of the internal clock signal.

15. (Original) The recapture circuit, according to claim 14, wherein the timing signal is a non-free running clock signal.

16. (Original) The recapture circuit, according to claim 14, wherein the timing signal is a strobe signal.

17. (Original) The recapture circuit, according to claim 16, wherein the internal clock signal and timing pulses of the strobe signal are at least approximately equal in frequency.

18. (Original) The recapture circuit, according to claim 16, wherein the internal clock signal and timing pulses of the strobe signal are out of phase.

19. (Original) The recapture circuit, according to claim 18, wherein the third plurality of registers is provided with a first-in, first-out buffer.

20. (Original) The recapture circuit, according to claim 14, wherein the timing signal is a free running clock signal.

21. (Original) The recapture circuit, according to claim 14, wherein the data

recapture stage further includes a fourth plurality of registers propagating the data valid signal to the third plurality of registers for write enabling the third plurality of registers.

22. (Original) A method for data recapture from a source synchronous interface, comprising:

obtaining a data signal via the source synchronous interface;

obtaining a timing signal via the source synchronous interface, the data signal and the timing signal being provided in association with one another;

dividing frequency of the timing signal to provide a derived timing signal;

capturing data of the data signal responsive to the timing signal and the derived timing signal, the data captured in a time domain of the timing signal;

generating a data valid signal from the derived timing signal and an internal clock signal, the data valid signal being internally timed without having to determine a system level delay; and

recapturing the data responsive to the internal clock signal and the data valid signal, the data recaptured being in a time domain of the internal clock signal.

23. (Original) The method, according to claim 22, wherein the capturing of the data comprises generating a plurality of data phases from the timing signal and the derived timing signal.

24. (Original) The method, according to claim 23, wherein the data valid signal generation comprises generating respective transfer done signals, wherein one of the transfer done signals leads the other of the transfer done signals.

25. (Original) The method, according to claim 24, wherein the transfer done signals are combined using a logical operator.

26.. (Original) The method, according to claim 25, wherein the logical operator is an OR operator.

27. (Original) An apparatus for data recapture from a source synchronous interface, comprising:

means for obtaining a data signal via the source synchronous interface;

means for obtaining a timing signal via the source synchronous interface, the data signal and the timing signal being provided in association with one another;

means for dividing frequency of the timing signal to provide a derived timing signal;

means for capturing data of the data signal responsive to the timing signal and the derived timing signal, the data captured in a time domain of the timing signal;

means for generating a data valid signal from the derived timing signal and an internal clock signal, the data valid signal being internally timed without having to determine a system level delay; and

means for recapturing the data responsive to the internal clock signal and the data valid signal, the data recaptured being in a time domain of the internal clock signal.

28. (Original) A recapture circuit, comprising:

a data capture stage including:

a first plurality of registers, the first plurality of registers coupled to receive a data signal and a timing signal and configured to capture data into a clock domain of the timing signal;

a frequency divider coupled to receive the timing signal and configured to provide an enable signal, the enable signal having a frequency less than the frequency of the timing signal;

the first plurality of registers coupled to receive the enable signal;

the first plurality of registers configured to provide a plurality of data phases, each of the data phases active on one of a leading edge or a lagging edge of the timing signal and one of high state or low state of the enable signal;

a data validity stage including:

a second plurality of registers, an input portion of the second plurality of registers coupled to receive the enable signal and an internal clock signal and configured to clock off of different phases of the internal clock signal, an output portion of the second plurality of registers coupled in series to the input portion and configured to clock off of different phases of the internal clock signal different from the input portion clockage;

a logical operator coupled to receive output from the second plurality of registers and configured to provide a data valid signal therefrom; and

a data recapture stage including:

a third plurality of registers, the third plurality of registers clocked responsive to the internal clock signal and write enabled responsive to the data valid signal, the third plurality of registers coupled to the first plurality of registers to receive output data therefrom and configured to recapture the output data into a clock domain of the internal clock signal.

29. (Original) The recapture circuit, according to claim 28, wherein the phases of the internal clock signal provided to the input portion of the second plurality of registers are 0 and 180 degrees.

30. (Original) The recapture circuit, according to claim 29, wherein the phases of the internal clock signal provided to the output portion of the second plurality of registers are 90 and 270 degrees.

31. (Original) The recapture circuit, according to claim 29, further comprising a digital clock module coupled to receive the internal clock signal and configured to provide the internal clock signal with the phases of 0, 90, 180 and 270 degrees.

32. (Original) The recapture circuit, according to claim 28, wherein the third plurality of registers is provided with at least one first-in, first-out buffer.